

Abstract of the Disclosure

The number of rewrites for memory cells is to be increased, and the reliability of data reading to be substantially improved. Where data in memory cells are to be erased, the switching of an erase voltage to be applied to the control gate of each memory cell, while switching from one to another of voltages of any different levels, as the control gate voltage (= soft erase voltage) is accomplished according to the quantity of electric charges accumulated at the floating gate of each memory cell so as to keep substantially constant the voltage applied to the tunnel film of the memory cell. Upon acceptance of an erase command, a CPU supplies a control signal to a decoder, and on the basis of the resultant decode signal an erase voltage switching circuit generates a soft erase voltage of a certain level. After that, while switching from one to another of soft erase voltages differing in level, data in the memory cell are erased. Upon completion of erasing data in the memory cell, erase verification is carried out.